CLAIMS

What is claimed is:

1. A method of fabricating an FET device comprising the steps of:
forming a semiconductor structure comprising a source region, a drain region over a horizontal surface of a substrate comprising an insulating material;
forming a channel structure over the horizontal surface of the substrate connecting between the drain region and the source region, with the channel structure comprising a horizontal semiconductor channel fin above a vertical fin with the planar fin and the vertical fin having a T-shaped cross-section, the vertical fin having a proximal edge and a distal edge, with the proximal edge in contact with the horizontal surface of the substrate and with the planar fin in contact with the distal edge of the vertical fin;
forming a gate dielectric layer over exposed surfaces of the channel structure; and forming a gate electrode straddling the channel gate dielectric and the channel structure.

2. The method of claim 1 wherein the channel structure comprises a vertical fin and a planar fin both composed of a semiconductor material.

3. The method of claim 1 wherein the channel structure comprises a vertical fin composed of an insulating material and a planar fin composed of a semiconductor material.

4. The method of claim 1 including the steps as follows:
forming a sacrificial layer over the horizontal surface of the substrate prior to forming the channel structure;

forming a patterned window extending through the sacrificial layer down to the horizontal surface of the substrate for shaping the vertical fin of the channel structure;
depositing a semiconductor layer filling the patterned window to form the vertical fin of the channel structure and forming a blanket semiconductor layer covering the sacrificial layer;
forming a channel mask over the blanket semiconductor layer aligned with the vertical fin of the channel structure;
etching away portions of the blanket semiconductor layer aside from the channel mask to form the planar fin;
whereby the channel structure comprises a vertical fin and a planar fin.

5. The method of claim 4 wherein the vertical fin and a planar fin are both composed of silicon.

6. The method of claim 4 wherein the vertical fin and a planar fin are both composed of a material selected from Ge and SiGe.

7. The method of claim 4 wherein:
the semiconductor material comprises silicon (Si); and
the sacrificial layer comprises silicon-germanium (SiGe).

8. The method of claim 4 wherein:
the semiconductor material comprises a material selected from Ge and SiGe; and
the sacrificial layer comprises a material selected from silicon (Si) and SiC.

9. The method of claim 1 including the steps as follows:
forming a sacrificial layer over the horizontal surface of the substrate prior to forming the channel structure;

forming a patterned window extending through the sacrificial layer down to the horizontal surface of the substrate for shaping the vertical fin of the channel structure;
depositing a dielectric layer filling the patterned window to form the vertical fin of the channel structure and forming a blanket semiconductor layer covering the sacrificial layer;
forming a channel mask over the blanket semiconductor layer aligned with the vertical fin of the channel structure;
etching away portions of the blanket semiconductor layer aside from the channel mask to form the planar fin;
whereby the channel structure comprises a vertical dielectric fin and a planar semiconductor fin.

10. The method of claim 9 wherein the planar fin is composed of a material selected from silicon (Si), germanium (Ge) and SiGe.

11. The method of claim 9 wherein the planar fin is composed of silicon (Si) and the sacrificial layer is composed of SiGe.

12. The method of claim 9 wherein the planar fin is composed of SiGe and the sacrificial layer is composed of comprises a material selected from silicon (Si) and SiC.

13. The method of claim 9 wherein the vertical fin is composed of a material selected from silicon dioxide and silicon nitride.

14. An FET device comprising:
a semiconductor structure comprising a source region, a drain region over a horizontal surface of a substrate comprising an insulating material;

a channel structure over the horizontal surface of the substrate connecting between the drain region and the source region, with the channel structure comprising a horizontal semiconductor channel fin above a vertical fin with the planar fin and the vertical fin having a T-shaped cross-section, the vertical fin having a proximal edge and a distal edge, with the proximal edge in contact with the horizontal surface of the substrate and with the planar fin in contact with the distal edge of the vertical fin;

a gate dielectric layer over exposed surfaces of the channel structure; and

a gate electrode straddling the channel gate dielectric and the channel structure.

15. The FET device of claim 14 wherein the channel structure comprises a vertical fin and a planar fin both composed of a semiconductor material.

16. The FET device of claim 14 wherein the channel structure comprises a vertical fin composed of an insulating material and a planar fin composed of a semiconductor material.

17. The FET device of claim 14 wherein the vertical fin and a planar fin are both composed of silicon.

18. The FET device of claim 14 wherein the vertical fin and a planar fin are both composed of a material selected from Ge and SiGe.

19. The FET device of claim 14 wherein the vertical fin is composed of a dielectric and the planar fin is composed of a material selected from silicon (Si), germanium (Ge) and SiGe.

20. The FET device of claim 14 wherein the vertical fin is composed of a dielectric and the planar fin is composed of silicon (Si) and the sacrificial layer is composed of SiGe.